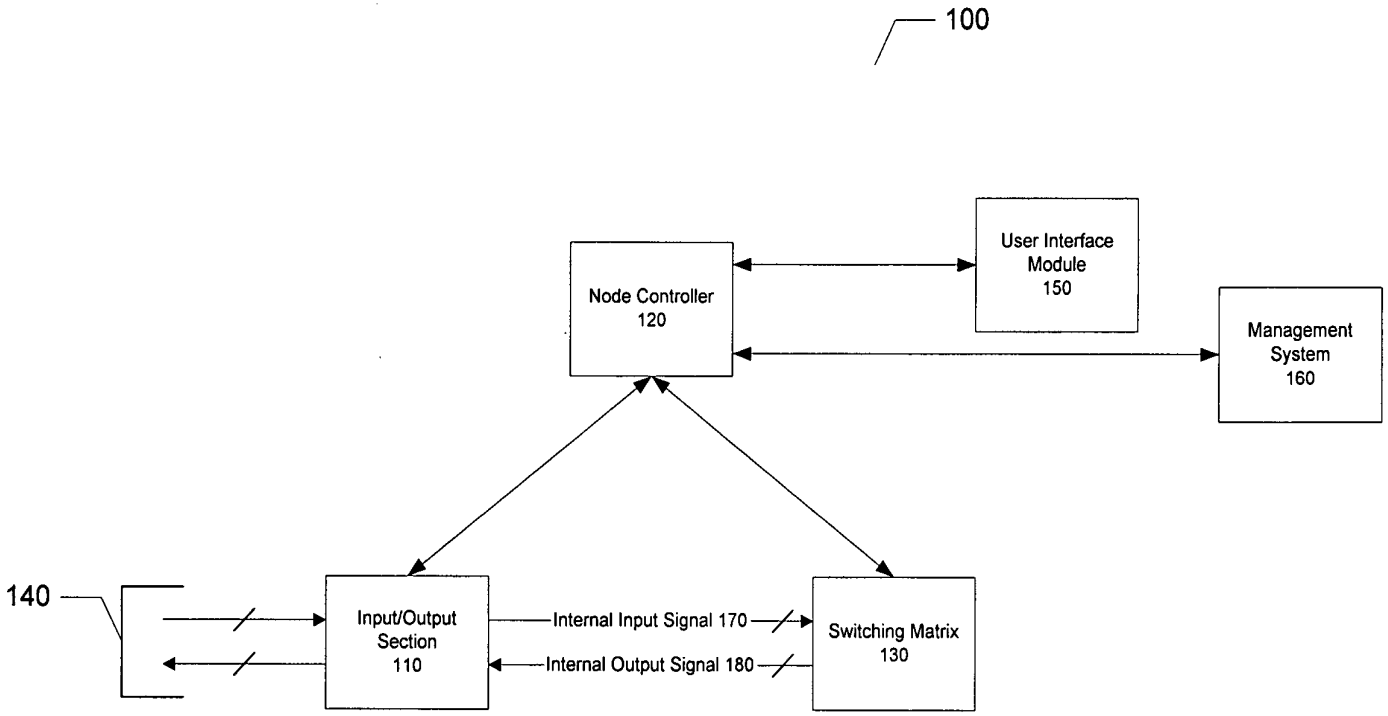
100
User Interface Module 150
Node Controller 120
Management System 160
140
Input/Output Section 110
Internal Input Signal 170
Internal Output Signal 180
Switching Matrix 130

Fig. 1A

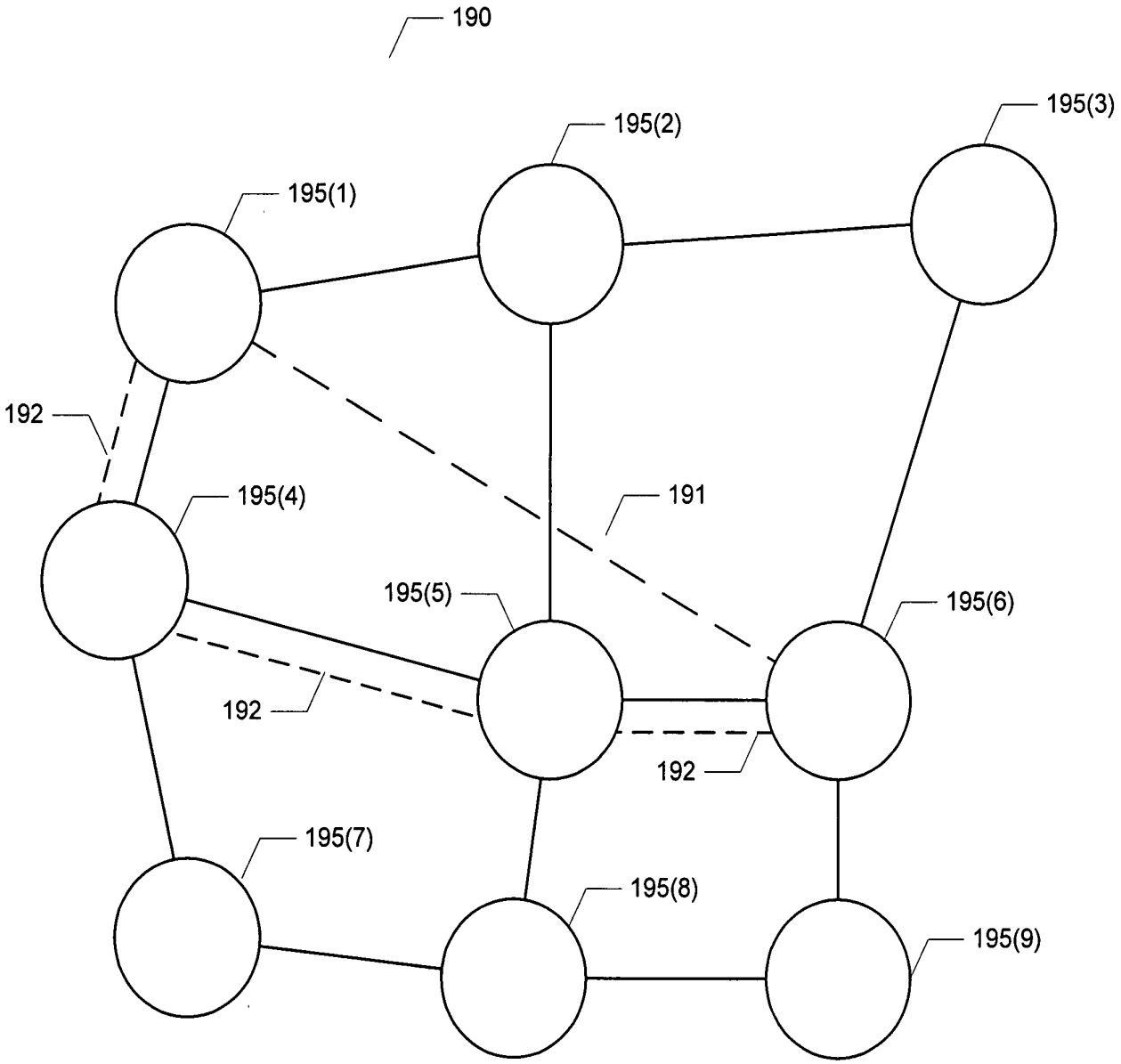
190
195(1)
195(2)
195(3)
192
195(4)
191
195(5)
195(6)
192
192
195(7)
195(8)
195(9)

Fig. 1B

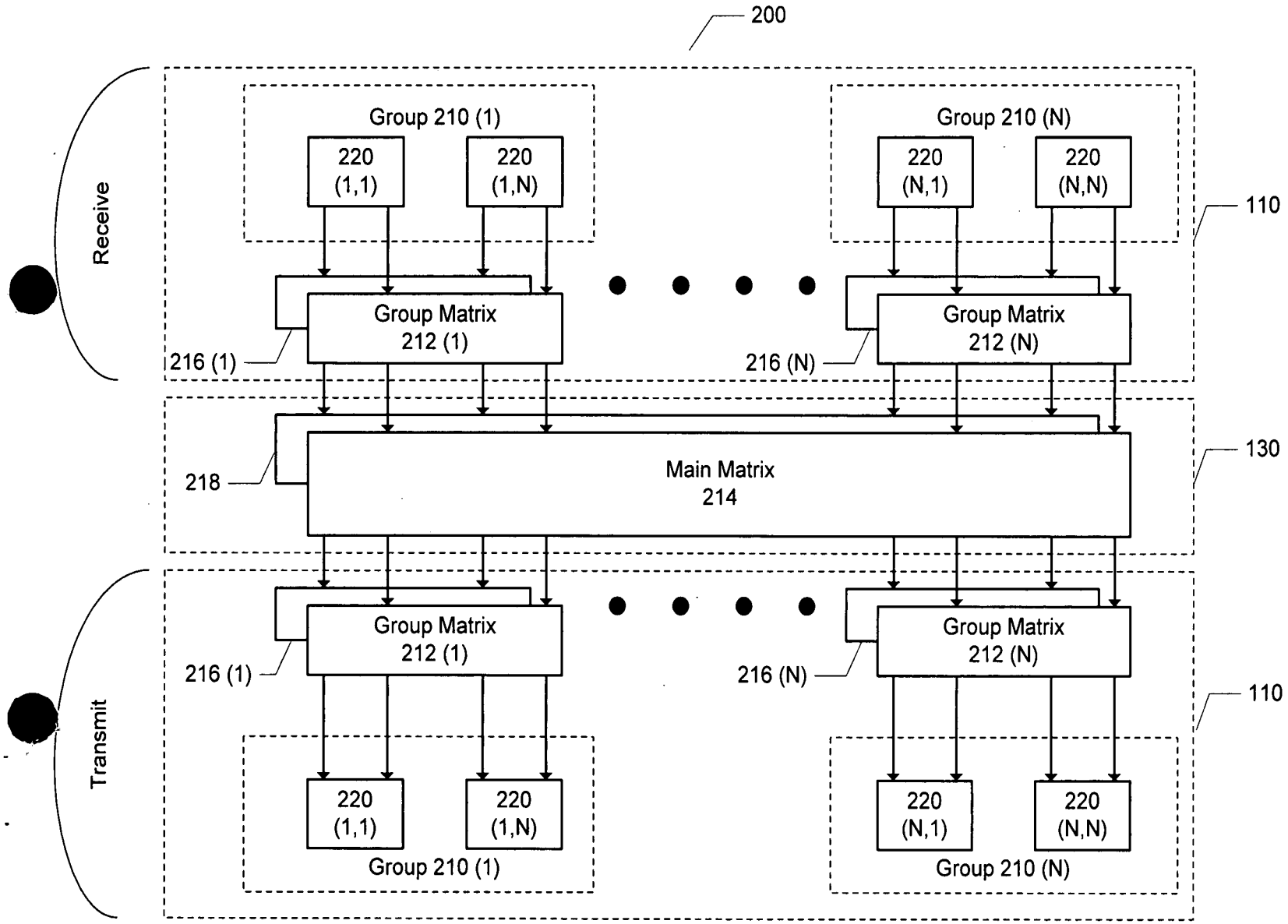
200
Receive
Group 210 (1)
220 (1,1)
220 (1,N)
Group 210 (N)
220 (N,1)
220 (N,N)
110
Group Matrix 212 (1)
216 (1)
Group Matrix 212 (N)
216 (N)
218
Main Matrix 214
130
Transmit
Group Matrix 212 (1)
216 (1)
Group Matrix 212 (N)
216 (N)
110
220 (1,1)
220 (1,N)
Group 210 (1)
220 (N,1)
220 (N,N)
Group 210 (N)

Fig. 2

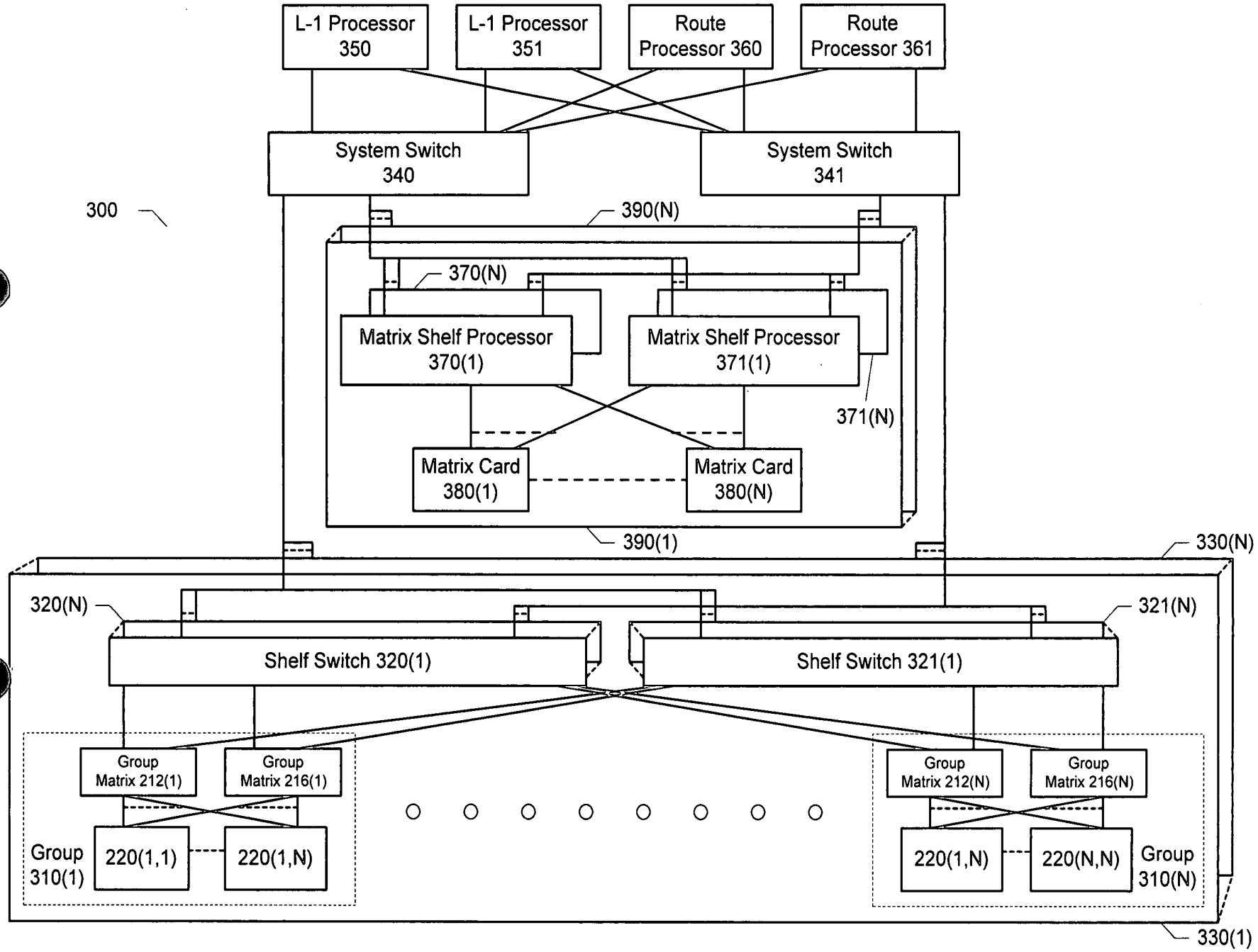
L-1 Processor 350
L-1 Processor 351
Route Processor 360
Route Processor 361
System Switch 340
System Switch 341
300
390(N)
370(N)
Matrix Shelf Processor 370(1)
Matrix Shelf Processor 371(1)
371(N)
Matrix Card 380(1)
Matrix Card 380(N)
390(1)
330(N)
320(N)
321(N)
Shelf Switch 320(1)
Shelf Switch 321(1)
Group Matrix 212(1)
Group Matrix 216(1)
Group Matrix 212(N)
Group Matrix 216(N)
Group 310(1)
220(1,1)
220(1,N)
220(1,N)
220(N,N)
Group 310(N)
330(1)

Fig. 3

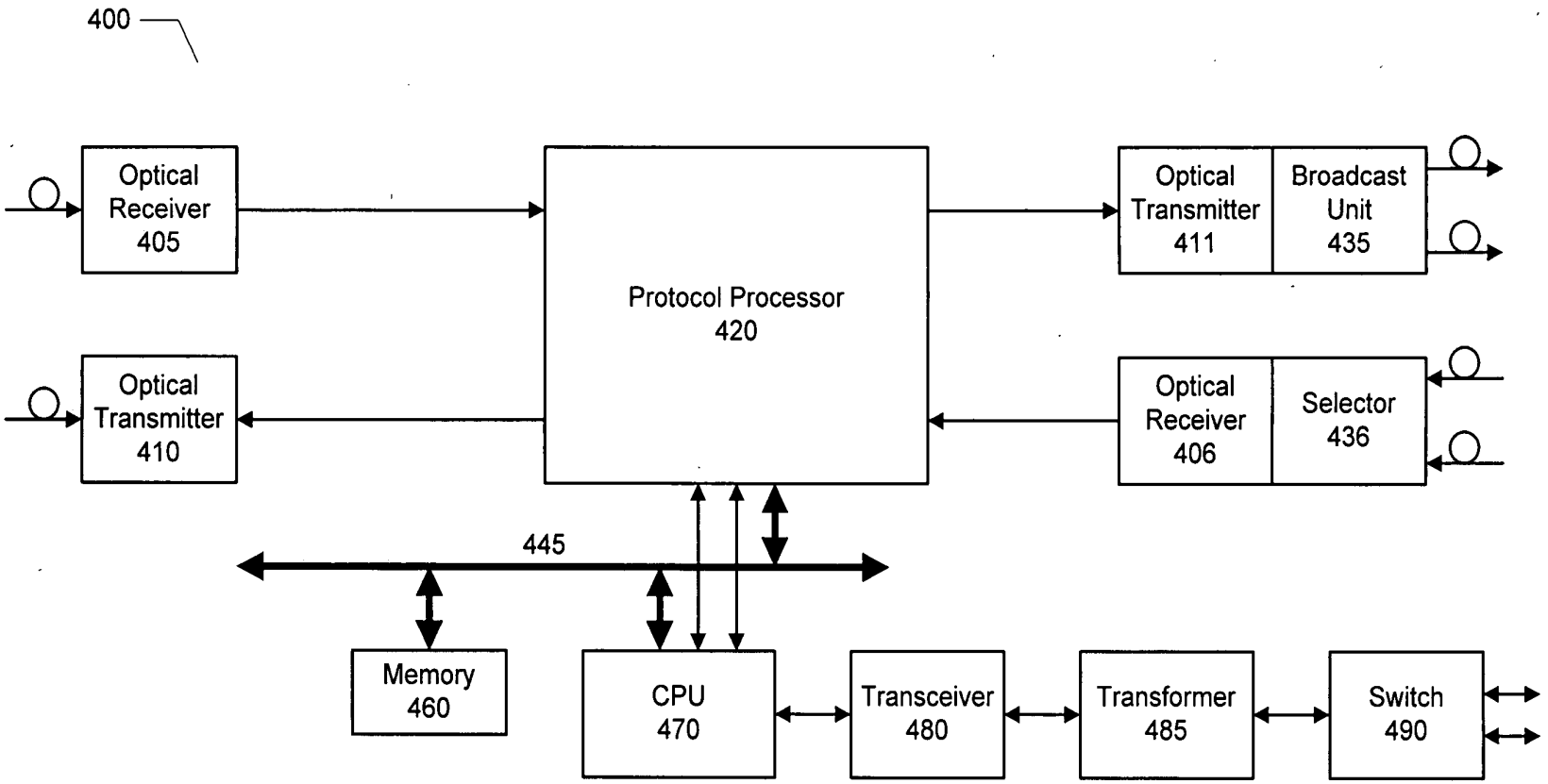
400
Optical Receiver 405
Protocol Processor 420
Optical Transmitter 411
Broadcast Unit 435
Optical Transmitter 410
Optical Receiver 406
Selector 436
445
Memory 460
CPU 470
Transceiver 480
Transformer 485
Switch 490

Fig. 4

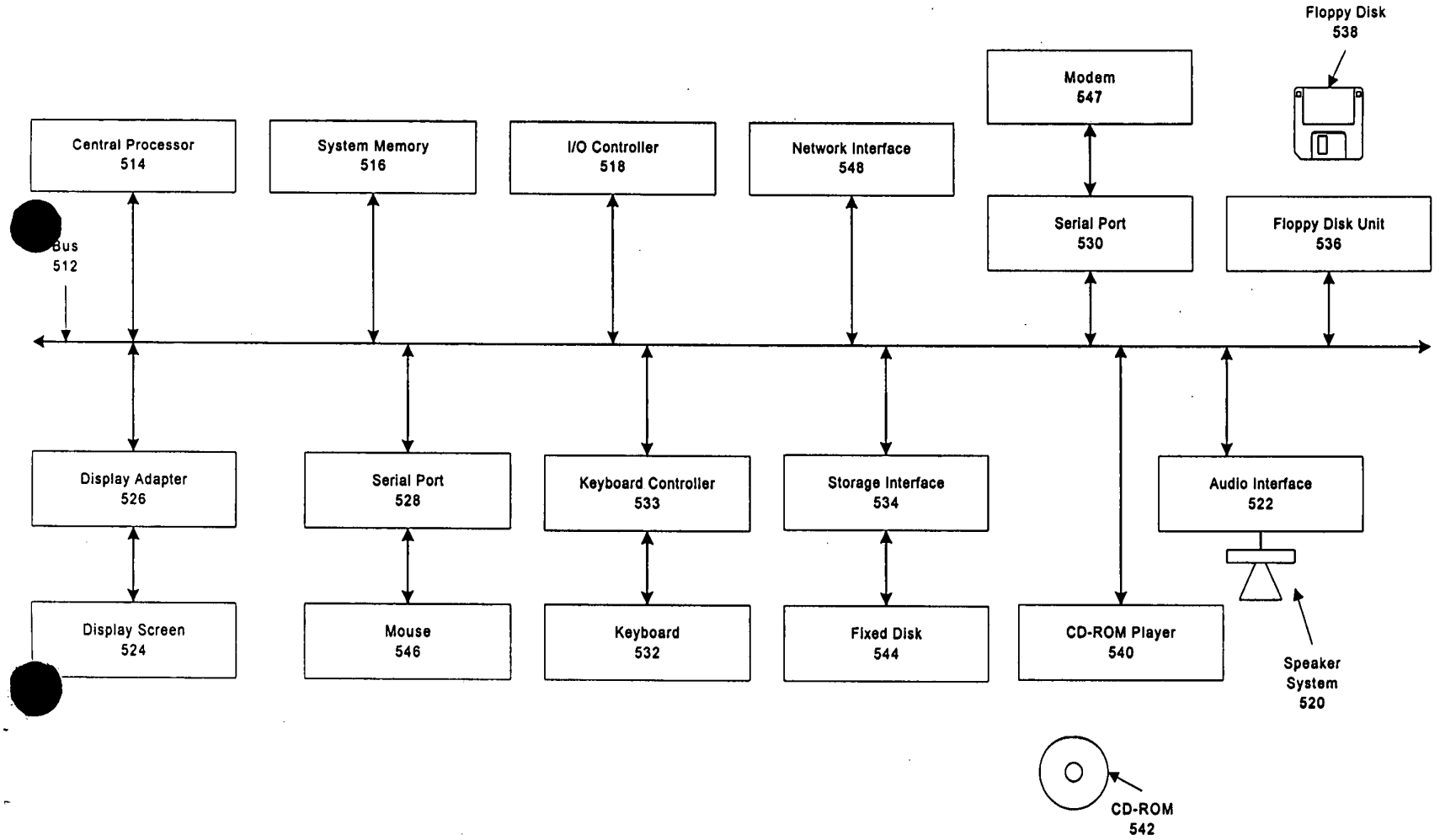
Floppy Disk
538
Modem
547
Central Processor
514
System Memory
516
I/O Controller
518
Network Interface
548
Serial Port
530
Floppy Disk Unit
536
Bus
512
Display Adapter
526
Serial Port
528
Keyboard Controller
533
Storage Interface
534
Audio Interface
522
Display Screen
524
Mouse
546
Keyboard
532
Fixed Disk
544
CD-ROM Player
540
Speaker
System
520
CD-ROM
542

Fig. 5

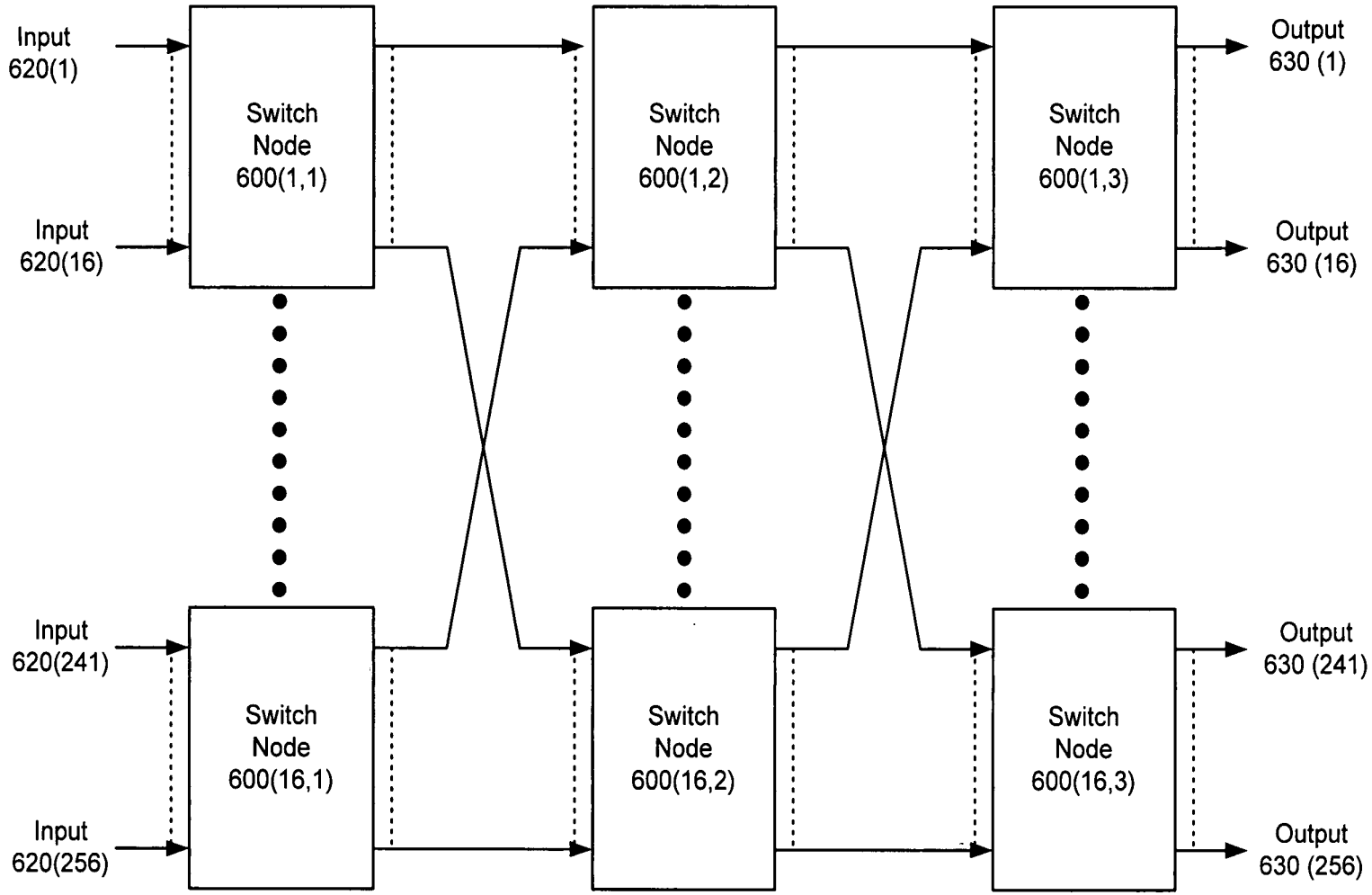
Input
620(1)
Input
620(16)
Input
620(241)
Input
620(256)
Switch
Node
600(1,1)
Switch
Node
600(1,2)
Switch
Node
600(1,3)
Switch
Node
600(16,1)
Switch
Node
600(16,2)
Switch
Node
600(16,3)
Output
630 (1)
Output
630 (16)
Output
630 (241)
Output
630 (256)

Fig. 6

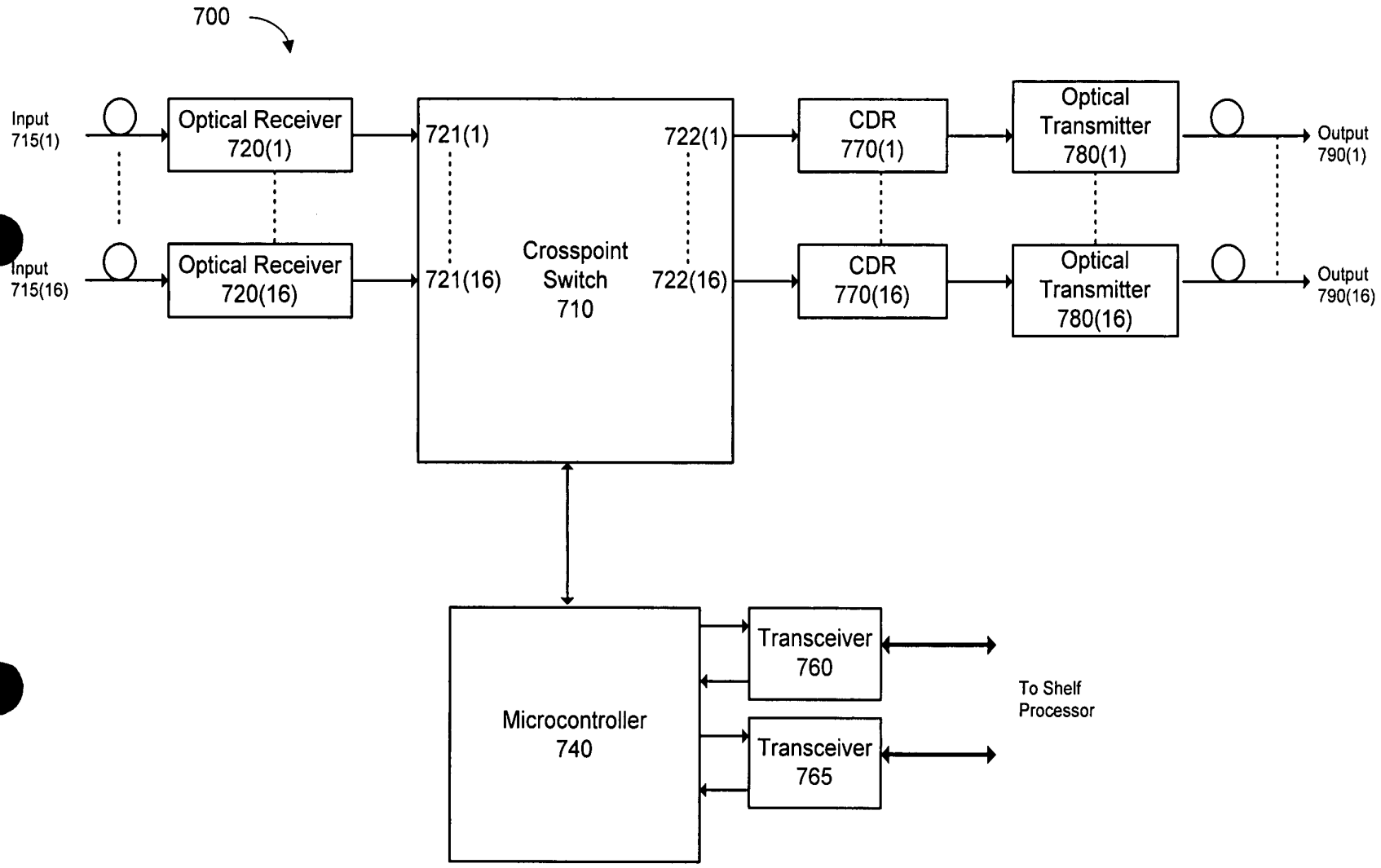
700
Input
715(1)
Optical Receiver
720(1)
721(1)
722(1)
CDR
770(1)
Optical
Transmitter
780(1)
Output
790(1)
Input
715(16)
Optical Receiver
720(16)
721(16)
Crosspoint
Switch
710
722(16)
CDR
770(16)
Optical
Transmitter
780(16)
Output
790(16)
Microcontroller
740
Transceiver
760
Transceiver
765
To Shelf
Processor

Fig. 7

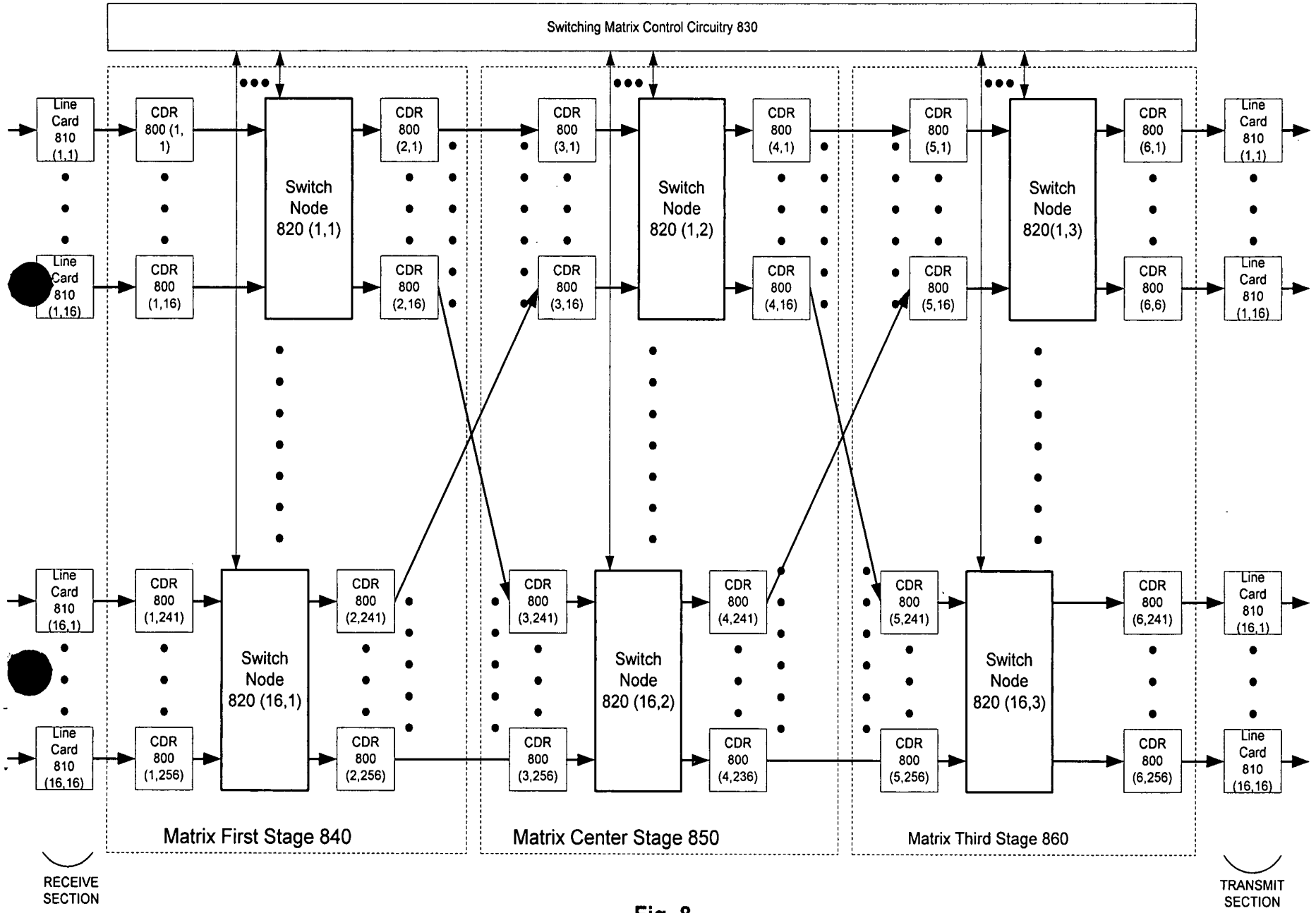
Switching Matrix Control Circuitry 830
Line Card 810 (1,1)
CDR 800 (1, 1)
Switch Node 820 (1,1)
CDR 800 (2,1)
CDR 800 (3,1)
Switch Node 820 (1,2)
CDR 800 (4,1)
CDR 800 (5,1)
Switch Node 820(1,3)
CDR 800 (6,1)
Line Card 810 (1,1)
Line Card 810 (1,16)
CDR 800 (1,16)
CDR 800 (2,16)
CDR 800 (3,16)
CDR 800 (4,16)
CDR 800 (5,16)
CDR 800 (6,6)
Line Card 810 (1,16)
Line Card 810 (16,1)
CDR 800 (1,241)
Switch Node 820 (16,1)
CDR 800 (2,241)
CDR 800 (3,241)
Switch Node 820 (16,2)
CDR 800 (4,241)
CDR 800 (5,241)
Switch Node 820 (16,3)
CDR 800 (6,241)
Line Card 810 (16,1)
Line Card 810 (16,16)
CDR 800 (1,256)
CDR 800 (2,256)
CDR 800 (3,256)
CDR 800 (4,236)
CDR 800 (5,256)
CDR 800 (6,256)
Line Card 810 (16,16)
Matrix First Stage 840
Matrix Center Stage 850
Matrix Third Stage 860
RECEIVE SECTION
TRANSMIT SECTION

Fig. 8

SONET Frame
900

A1 902	A2 904	J0/Z0 906 U	Payload Bytes 990	
B1 910	E1 912 U	F1 914 U	Payload Bytes 991	
D1 920 U	D2 922 U	D3 924 U	Payload Bytes 992	
H1 930	H2 932	H3 934	H4 936	Payload Bytes 993
B2 940 U	K1 942 U	K2 944 U	Payload Bytes 994	
D4 950 U	D5 951 U	D6 952 U	Payload Bytes 995	
D7 953 U	D8 954 U	D9 955 U	Payload Bytes 996	
D10 956 U	D11 957 U	D12 958 U	Payload Bytes 997	
S1/Z1 970 U	M1/Z2 972 U	E2 974 U	Payload Bytes 998	

Fig. 9
(Prior Art)

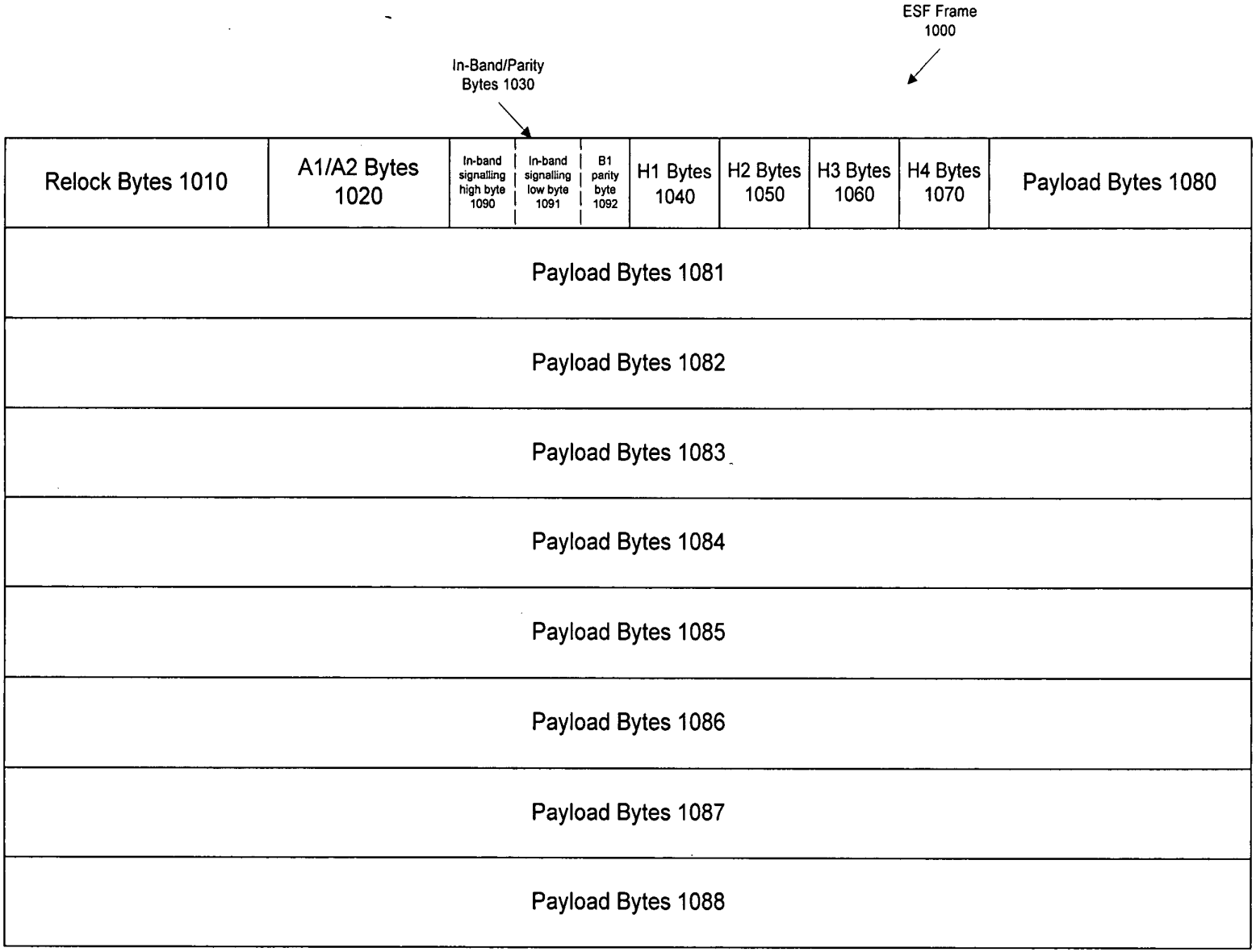
ESF Frame
1000
In-Band/Parity
Bytes 1030
Relock Bytes 1010
A1/A2 Bytes
1020
In-band
signalling
high byte
1090
In-band
signalling
low byte
1091
B1
parity
byte
1092
H1 Bytes
1040
H2 Bytes
1050
H3 Bytes
1060
H4 Bytes
1070
Payload Bytes 1080
Payload Bytes 1081
Payload Bytes 1082
Payload Bytes 1083
Payload Bytes 1084
Payload Bytes 1085
Payload Bytes 1086
Payload Bytes 1087
Payload Bytes 1088

Fig. 10

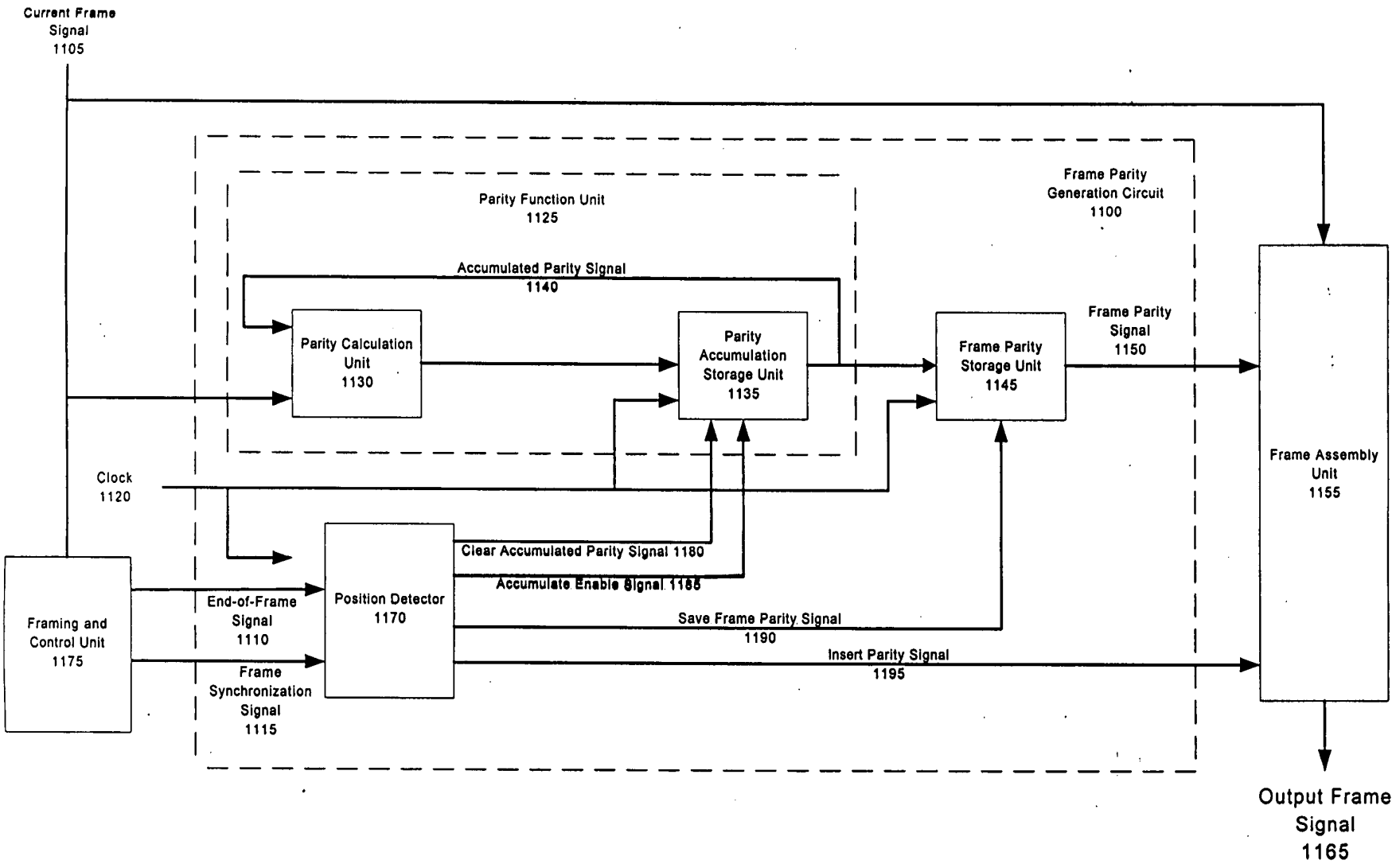

Fig. 11

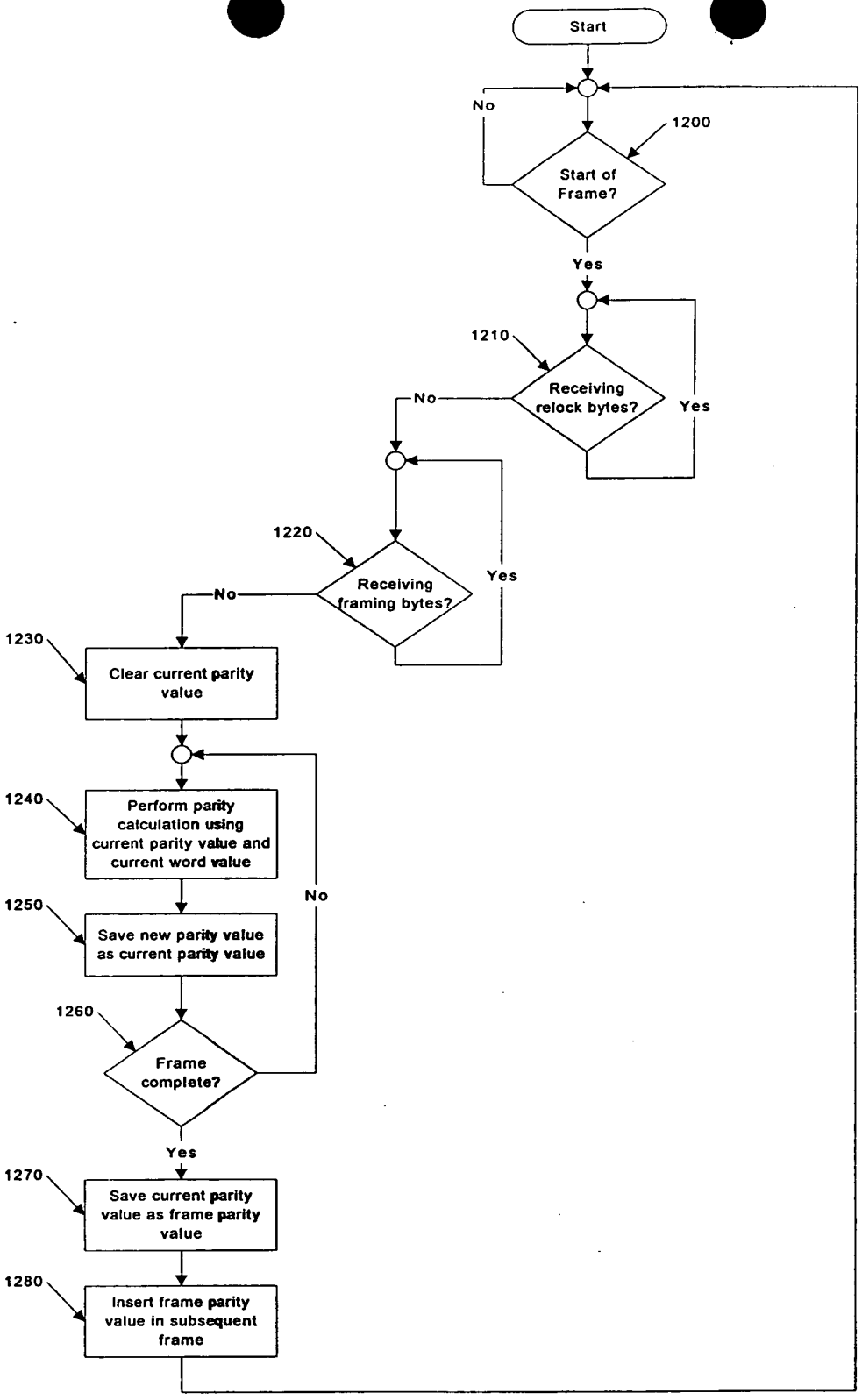
Start
No
1200
Start of Frame?
Yes
1210
Receiving relock bytes?
No
Yes
1220
Receiving framing bytes?
No
Yes
1230
Clear current parity value
1240
Perform parity calculation using current parity value and current word value
1250
Save new parity value as current parity value
1260
Frame complete?
No
Yes
1270
Save current parity value as frame parity value
1280
Insert frame parity value in subsequent frame

Fig. 12

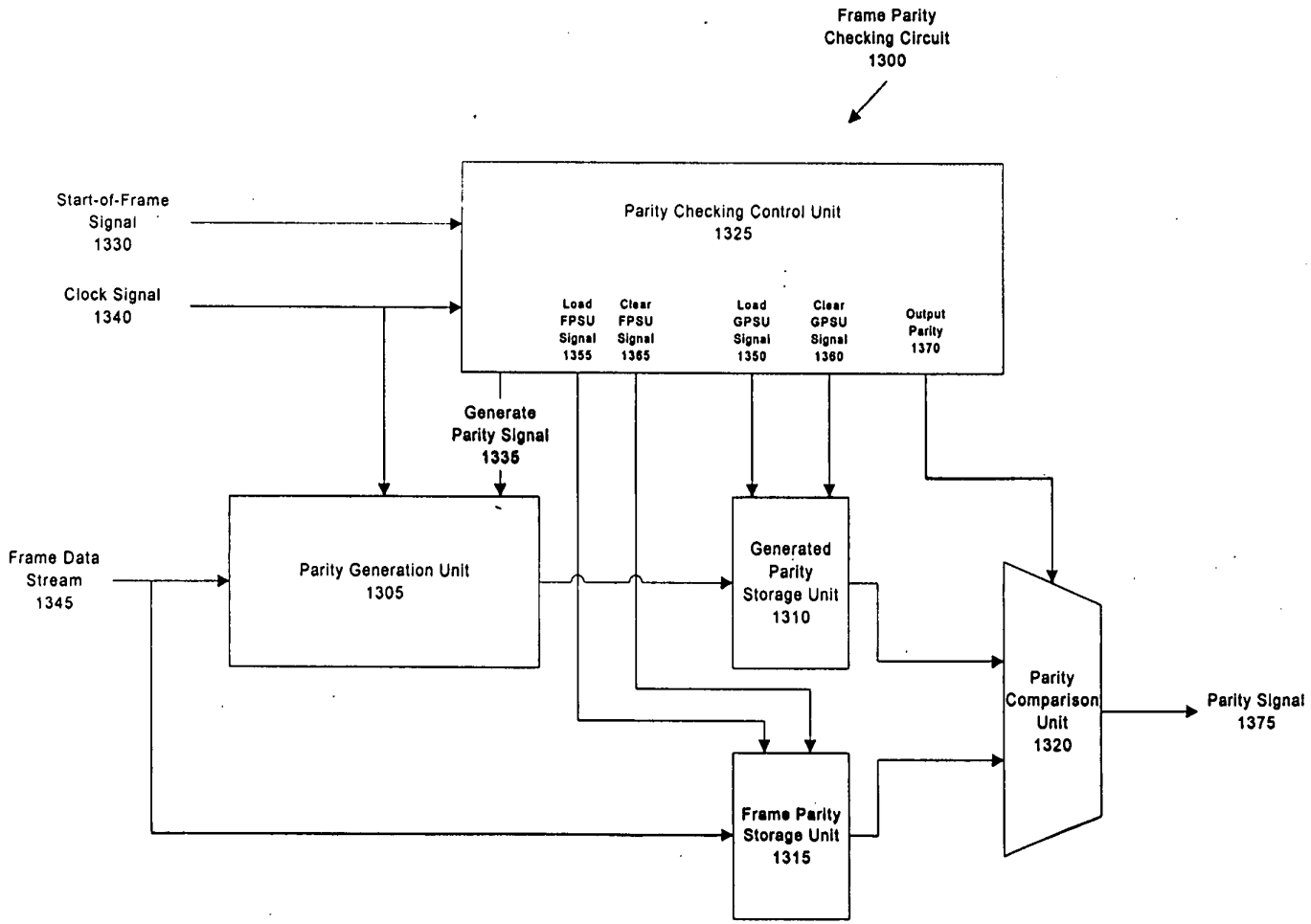
Frame Parity
Checking Circuit
1300
Start-of-Frame
Signal
1330
Clock Signal
1340
Parity Checking Control Unit
1325
Load
FPSU
Signal
1355
Clear
FPSU
Signal
1365
Load
GPSU
Signal
1350
Clear
GPSU
Signal
1360
Output
Parity
1370
Generate
Parity Signal
1335
Frame Data
Stream
1345
Parity Generation Unit
1305
Generated
Parity
Storage Unit
1310
Parity
Comparison
Unit
1320
Parity Signal
1375
Frame Parity
Storage Unit
1315

Fig. 13

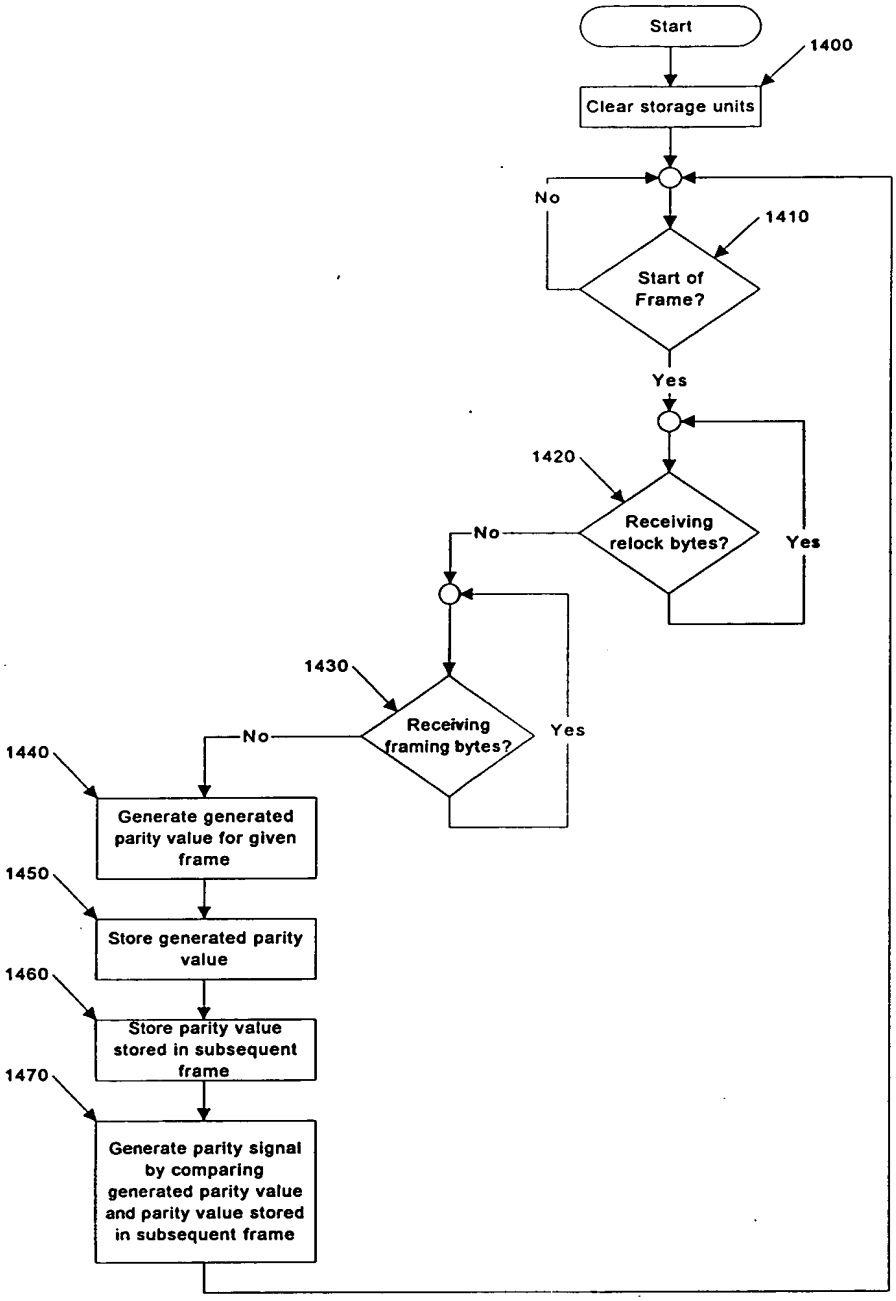
Start
1400
Clear storage units
No
1410
Start of Frame?
Yes
1420
Receiving relock bytes?
No
Yes
1430
Receiving framing bytes?
No
Yes
1440
Generate generated parity value for given frame
1450
Store generated parity value
1460
Store parity value stored in subsequent frame
1470
Generate parity signal by comparing generated parity value and parity value stored in subsequent frame

Fig. 14